CLAIMS:

1. A method of processing data of a data communication channel, comprising:

receiving a plurality of serial data signals from lanes of the communication channel;

de-multiplexing serial data from each of the serial data signals received from the lanes and formatting the data of the lanes into parallel data;

checking the parallel data for a start-of-frame (SOF) character;

responsive to the checking for a SOF character, parsing the parallel data into non-data and real data;

basing the parsing of the parallel data at least in part on placement relative to the SOF character;

packing the parsed real data into a group of data;

presenting the packed group of data; and

activating a start-of-frame sideband signal when beginning the presenting the packed group data.

2. The method of claim 1, further comprising:

checking the parallel data for an end-of-frame (EOF) character;

the parsing the parallel data to comprise determining if a character of the parallel data is outside a frame bounded by the SOF and the EOF characters, and if the character is determined outside the frame, defining the character as non-data.

3. The method of claim 2, the parsing further to define the SOF and EOF characters as non-data.

4. The method of claim 3, the parsing further to comprise:

checking for idle characters between the SOF and the EOF characters, and

responsive to the checking for idle characters, defining the idle characters as non-data.

5. The method of claim 2, in which the packing configures the real data into a contiguous group.

6. The method of claim 5, further comprising activating an end-of-frame sideband signal when sending out a last portion of the contiguous group.

7. The method of claim 6, in which the packing comprises aligning the real data of the contiguous group with one of a left or a right alignment relative to at least one of the SOF and EOF sideband signals.

8. The method of claim 2, in which

the receiving comprises receiving sequential words each having a byte width proportional to the number of lanes;

the checking for the EOF character comprises examining bytes in a first word including the SOF character; and

if the EOF character is not found, the method further comprising repeating for subsequent words the receiving,

de-multiplexing, parsing and packing until finding an EOF character.

9. The method of claim 8, in which the received sequential words comprise characters of left to right relationship corresponding to time-ordered placement of the characters.

10. The method of claim 8, further comprising performing at least one of storing and outputting data based on the number of characters previously packed, the amount of new real data packed during the repeating, and the size of the output.

11. The method of claim 10, in which the new real data is stored when the total real data is less than or equal the size of the output, and when the EOF character has not been found.

12. The method of claim 11, in which a portion of the new real data is output together with previously packed data, and a remaining portion of the new real data is stored when the total real data exceeds the size of the output.

13. The method of claim 11, in which the packed data is output when an EOF character has been found.

14. The method of claim 1, further comprising:

identifying a number of lanes in the communication channel; and

configuring serial-to-parallel data receivers to receive and de-multiplex the serial data signals of the identified lanes to form output characters for the parallel data.

15. A circuit to interface a communications channel comprising:

a plurality of serial-to-parallel receivers to receive serial data signals of data lanes of the communications channel and recover characters of parallel format from the data lanes;

a plurality of decoders to determine character types of the characters recovered by the receivers of the data lanes;

detectors to detect at least one of a start-of-frame (SOF) character and an end-of-frame (EOF) character;

parser to parse characters recovered by the receivers based on the character types determined by the decoders and placement relative to a detected SOF character; and

a packer to group the parsed characters.

16. The circuit of claim 15, in which the decoders resolve character types of the group consisting of at least one of SOF, EOF, real data and idle data characters; and

the parser to invalidate characters determined to be outside a frame delineated by at least one of a detected SOF character and a detected EOF character.

17. The circuit of claim 16, in which the packer is operable to pack decoded real data characters of the characters determined inside the frame, and to align the packed data characters with one of a left of right alignment.

18. The circuit of claim 17, the parser and the packer further to group the packed data characters into a contiguous block, the contiguous block having no idle characters between real data characters.

19. The circuit of claim 17, further comprising:

storage registers accessible to store characters for subsequent retrieval; and

a storage controller to transfer the aligned data characters to the storage registers if the detectors determine absence of an EOF character.

20. The circuit of claim 19, further comprising:

a data output port having a word width; and

in which the storage controller is further operable to determine a first amount of the aligned data characters, a second amount of data characters retained in the storage registers, and if a total of the first and second amounts is greater than the word width of the output port, to transfer at least a portion of the aligned data characters to the storage registers.

21. The circuit according to claim 20, further comprising an output controller to enable transfer of data characters to the output port responsive to at least one of the detector detecting an EOF character and the storage controller determining that the total is at least equal to the word width of the output port.

22. The circuit of 21, in which the storage controller and output controller are further operable, responsive to determining the total is greater than the word width of the output port, to take characters from the storage registers and a portion of the aligned data characters to form and present an output word on the output port.

23. The circuit of 22, in which the storage controller and output controller are further operable to write a remaining portion of the aligned real characters into the storage registers.

24. A system to interface a communication channel having a plurality of serial data lanes, comprising:

a plurality of receivers to receive the serial data from the data lanes, each receiver comprising a serial-to-parallel converter to convert received serial data to parallel format;

the plurality of receivers comprising outputs that collectively form a word having a width related to the number of data lanes;

decoders to identify character types recovered by the receivers;

logic to determine when a decoder of the decoders has identified at least one of the character types of the group consisting of a start-of-frame and an end-of-frame character;

parsing circuitry to determine valid characters of the word based upon placement relative to the identified start-of-frame character and the end-of-frame character;

a storage register selectively operable to receive characters that have been determined valid by the parser; and

a controller to control presentment of determined valid data to at least one of the storage registers or an output port, the presentment based on character types identified by the decoders, the placements relative the SOF character, a first amount of the valid characters determined by the parsing circuitry, and a second amount of characters stored in the storage registers.

25. The system of claim 24, further comprising a generator to present a sideband start-of-frame signal to accompany valid data at the output port when first presented.

26. The system of claim 25, the generator further to present a sideband end-of-frame signal to accompany parsed valid data at the output port when the decoder and the logic have determined an EOF character and the controller enabled presentment of valid data of a word associated with the EOF character.

27. The system of claim 26, the generator to further present a data valid signal when parsed valid data and the accompanying EOF sideband signal are presented at the output port.

28. The system of claim 24, the logic further operable to determine which of the decoders have identified real-data character types and those that have identified idle character types.

29. The system of claim 28, further comprising alignment circuitry to align the real-data characters into a contiguous block with one of a left or right alignment relative to a delineated between the SOF and the EOF characters.

30. The system of claim 29, in which the controller is operable to store the aligned data characters in the storage registers when the total of the amount of aligned characters and the amount of characters in the storage register is less than or equal the width of the output port.

31. The system of claim 30, in which the controller is further operable to store a remaining portion of the aligned data characters in the storage register when the total exceeds the width of the output port.

32. The system of claim 30, in which the controller is operable to output the stored characters of the storage registers responsive to the decoders and the logic determining an EOF character.

33. The system of claim 28, in which

at least a portion of the receivers, the decoders, the logic, the parsing circuitry, the storage registers, and the controller comprise devices embedded within a programmable logic device; and

another portion thereof comprise configured programmable resources of the programmable logic device.

34. The system of claim 33, in which the programmable logic device comprises configuration memory programmed with configuration data operable to configure the programmable resources adaptive to the number of serial data lanes of the communication channel.

35. The system of claim 33, in which the decoders comprise content addressable memories embedded within the programmable logic device and configurable per the programmable resources of the programmable logic device to receive characters of the receiver outputs and to source decode information to the logic.

36. A circuit to interface to a communications channel comprising:

means for receiving data signals from data lanes of a communication channel;

de-multiplexing means for recovering serial data from the data signals and converting the serial data into parallel data;

decode means for decoding characters recovered by the de-multiplexing means;

detection means for detecting at least one of a start-of-frame (SOF) character and an end-of-frame (EOF) character;

parser means for parsing characters based on type decoded and placement relative to a SOF character; and

means for grouping together parsed characters.

37. The circuit of claim 36, in which the decode means resolves character types of the group consisting of at least one of SOF, EOF, real data and idle data characters; and

the parser means further bases the parsing upon whether the character placement is outside a frame delineated by at least one of a detected SOF character and a detected EOF character.

38. The circuit of claim 37, in which the grouping means groups real data characters determined inside the frame with one of a left of right alignment.

39. The circuit of claim 38, the parser means and the grouping means to group the data characters into a contiguous block having no idle characters.